Docket No. 37213-01000
Express Mail Label No. EL 705 882 978US

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

U.S. NON-PROVISIONAL PATENT APPLICATION

FOR

DEVICE AND METHOD FOR SIGNAL PROCESSING

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DEVICE AND METHOD FOR SIGNAL PROCESSING

FIELD OF THE INVENTION

The present invention relates to signal processing technology and, more particularly, to devices and methods for processing digital signals such as, for example, digital audio signals.

BACKGROUND OF THE INVENTION

It has been documented that a digital-to-analog converter may be used to process digitized signals for amplification by an analog power amplifier. For example, Erik Bresch and Wayne T. Padgett in "TMS320C67-Based Design Of A Digital Audio Power Amplifier Introducing Novel Feedback Strategy" (http://www.ti.com/sc/docs/general/dsp/fest99/poster/hbreschpadgett.pdf) describe such an amplification technique used in connection with audio signals. FIG. 1 shows a basic structure of a Class-D type audio power amplifier as depicted by Bresch and Padgett.

Certain digital audio signal sources, such as compact disk (CD) players, provide digitized audio signals that are pulse code modulated. Such digitized audio signals may have a 16-bit resolution and a 44.1 kHz sampling frequency. However, the audio signal may need to be modulated and amplified to be useful in particular applications.

A number of techniques allow a digital data stream to be represented as an analog signal. One such technique includes the use of a sigma-delta modulator, and another technique includes employing a pulse width modulator.

Each of these two techniques has certain advantages and disadvantages for particular applications. For example, output from a sigma-delta modulator may have a

high degree of accuracy such that the amount of noise is relatively low and the amount of total harmonic distortion (THD) is favorable (perhaps about 0.001%) for certain audio equipment applications. As documented by James Candy and Gabor Temes in "OverSampling Delta-Sigma Data Converters" (ISBN 0-87942-285-8), one conventional technique used in certain sigma-delta modulators is to convert a stream of 16-bit audio data into a stream of 4-bit data at a higher clock rate. It has also been documented that the noise associated with such a quantization to 4-bits may be "shaped" so that it all appears in relatively high frequencies. However, one disadvantage of such a technique (at least for certain audio equipment applications) is that digital output from a sigma-delta modulator may not be easily converted into an analog voltage due to variable frequencies present in the data stream.

A pulse width modulator may produce an output with a low and controlled frequency that may be able to drive a Class-D type audio power amplifier and be relatively easily converted into an analog voltage. In addition, certain pulse width modulation techniques may introduce less error than certain sigma-delta modulation techniques.

Certain developers have tried to produce a signal with the positive distortion and noise performance characteristics of a sigma-delta modulation technique, as well as the low frequency and predicable output characteristics of a pulse-width-modulation technique. For example, Bresch and Padgett have documented one such attempt in "TMS320C67-Based Design of a Digital Audio Power Amplifier Introducing Novel Feedback Strategy." In addition, it has been documented by K.P. Sozaski, R. Strzelecki and Z. Fedyczak in "Digital Control Circuit for Class-D Audio Power

Amplifier" that an attempt to combine a sigma-delta type modulator with a pulse width modulator resulted in a signal-to-noise ratio that approached 75 db in the audio frequency band (i.e., 20 Hz to 20 kHz). However, such performance may be insufficient or unacceptable in certain circumstances or for particular users.

Recognizing that a pulse width modulator may introduce distortion (which is thought to be caused by a high harmonics content in the audio frequency band) into a signal such as an audio signal, certain developers have tried to reduce the distortion by (1) using a sigma-delta-to-pulse-width-modulator circuit to create an analog output, and then (2) feeding back that analog output in a closed loop system to create an error signal. U.S. Patent No. 6,515,604 to Delano discusses such a system to create an error signal. Bresch and Padgett discuss another system of this type in "TMS320C67-Based Design of a Digital Audio Power Amplifier Introducing Novel Feedback Strategy."

For certain applications or users, however, it may be desirable to correct for distortion in the digital domain. In addition, it may be desirable at least for particular audio equipment applications to have a signal processor capable of a high degree of noise shaping similar to a sigma-delta modulator. Additional favorable characteristics of such a signal processor may include both a modulation depth such that large signal amplitudes may be generated in a particular frequency range (e.g., the audio frequency range), as well as the use of a relatively small and fixed number of values for a given time period such that a simple digital to analog converter can be made using, for example, an RC network connected to a simple digital driver. Yet another desirable characteristic of such a signal processor may be a low output frequency so that it can be used to drive switches (e.g., MOSFETs) of the type used in certain Class-D type audio power amplifiers.

SUMMARY OF THE INVENTION

In one aspect, the invention features a signal processor with a pulse width modulator that has a clock rate. The signal processor of this aspect also includes a digital filter configured to receive an output of the pulse width modulator, wherein the output includes distortion and wherein the digital filter samples the output at the clock rate to suppress the distortion.

In another aspect, the invention features a digital circuit for suppressing distortion in a digital signal that exists after a pulse width modulation, wherein the pulse width modulation occurs at a clock rate, and wherein the digital circuit includes a digital filter configured to receive the signal having the distortion and to sample the signal at the clock rate.

In a further aspect, the invention features a digital signal processing circuit including a pulse width modulator having an output with a distortion, the circuit further including means for sampling the output and suppressing the distortion in a digital domain.

In yet another aspect, the invention features a signal processor for modulating a digital input signal. The processor of this aspect includes a closed loop digital circuit having a forward path with a filter coupled with and upstream from an encoder stage, wherein the encoder stage has a first order sigma-delta type modulator and a pulse width modulator. In such an aspect, the sigma-delta type modulator generates an oversampled signal that has a period and a total number of levels, and the pulse width modulator operates at a clock rate that is M times the period, where M is the total number of levels in the oversampled signal, and wherein the forward path produces an output and

a distortion. Also, in such an aspect, the processor further includes a feedback path that has a low pass single pole IIR filter that samples the output in a digital domain to suppress the distortion.

In another aspect, the invention features a signal processor that includes an oversampling circuit coupled with a pulse width modulation circuit that has an output. In this aspect, the signal processor also includes a feedback path with a digital filter that samples the output in a digital domain.

In a further aspect, the invention features an integrated circuit chip configured to receive a pulse code modulated digital signal and to generate a pulse width modulated digital signal having a distortion, wherein the distortion is suppressed by a digital filter that operates at a clock rate of the pulse width modulated digital signal.

In still another aspect, the invention features a method including modulating a first pulse code modulated signal having a first resolution into a second pulse code modulated signal having a second resolution, wherein the second resolution is smaller than the first resolution. In such an aspect, the method also includes modulating the second pulse code modulated signal into a third signal that has a plurality of pulses in time generated at a clock rate, and further includes filtering in a digital domain the plurality of pulses in time to suppress a distortion in the third signal.

In a further aspect, the invention features a device that includes means for modulating a first pulse code modulated signal having a first resolution into a second pulse code modulated signal having a second resolution, wherein the second resolution is smaller than said first resolution. In such an aspect, the device further includes means for modulating the second pulse code modulated signal into a third signal having a plurality

of pulses in time having a clock rate, as well as means for filtering in a digital domain the plurality of pulses in time to suppress a distortion in the third signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features and other aspects of the invention are explained in the following description taken in connection with the accompanying drawings, wherein:

FIG. 1 depicts a block diagram of a conventional structure of a Class-D audio amplifier, as documented by Bresch and Padgett;

FIG. 2 depicts a block diagram of an embodiment of a signal processor 200 according to the present invention;

FIG. 3 depicts a block diagram of a digital power amplification system 300 according to an embodiment of the present invention;

FIGS. 4a and 4b depict a block diagram of a method of modulating and amplifying a digital signal according to an embodiment of the present invention;

FIGS. 5a and 5b depict simplified integrated circuit chips 501, 510 according to embodiments of the present invention;

FIG. 6 depicts a portable audio player 600 according to one embodiment of the present invention; and

FIGS. 7a – 7d depict a computer code listing of Verilog modules representing one embodiment of the present invention.

FIG. 8 depicts a frequency response plot for a computer model of one embodiment of the present invention.

FIG. 9 depicts a frequency response plot for a computer model of another embodiment of the present invention.

FIG. 10 depicts a frequency response plot measured using an FPGA implementation of the embodiment used to produce the plot shown in FIG. 9.

It is to be understood that the drawings are exemplary, and are not to be deemed limiting to the full scope of the appended claims.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Various embodiments of devices, systems and methods in accordance with embodiments of the present invention will now be described with reference to the drawings.

In one embodiment of the present invention, a signal processor 200 receives a digital wide-bit input signal and uses feedback that is entirely in the digital domain to correct for any error that may be introduced into the output signal 235 by the process of pulse width modulating the input signal 205. Various embodiments of the present invention may include, for example, (1) an integrated circuit chip 501 for use in an optical disk player (e.g., a digital versatile disk (DVD) player), wherein the chip 501 contains at least two signal processors 200-1, 200-2 (i.e., one for left channel output and the other for right channel output), (2) an integrated circuit chip 551 for use in a surround sound audio power amplifier, wherein the chip 551 may contain eight signal processors 200-1 to 200-8 (i.e., one for each of eight output channels), (3) a portable electronics player 600, which may have headphones, wherein at least one signal processor 200 is used in connection with a digital power amplification system 300 such as, e.g., a headphone amplifier; (4) a general purpose digital-to-analog converter such as may be used in an industrial automation system (e.g., a 16-bit digital-to-analog converter), and

(5) an integrated circuit chip for use in telecommunications equipment (e.g., a mobile or cellular phone).

As depicted in FIG. 2, one embodiment of the present invention features a closed loop signal processor 200 which implements a digital filter 240 that samples a pulse width modulated output signal 235 entirely in the digital domain to thereby assess and correct for distortion. In particular, FIG. 2 depicts a block diagram of a closed loop signal processor 200 according to one embodiment of the invention. In this embodiment, a digital input signal 205 is sent through a forward path that includes an integrator stage 220 and an encoder stage 230, and is augmented by a fully digital feedback path that closes the control circuit of the embodiment. The digital input signal 205 may be, for example, a 16-bit pulse code modulated signal at a 44.1 kHz frequency. A digital filter 240 of the embodiment shown in FIG. 2 may help capture distortion created by the encoder stage 230 (and, more specifically, distortion created by the conversion technique of an embodiment that has an oversampling filter 232 to pulse width modulator 234 combination) because the digital filter 240 of the embodiment samples each of the sub-intervals of the pulse width modulated signal 235 and uses a low pass filter to smooth the pulse width modulated digital signal 235 datastream.

The filter stage 220 of one embodiment may be a single digital integrator (i.e., a single pole filter with a origin pole). In such an embodiment, the filter stage 220 receives and accumulates any difference there may be between the digital input signal 205 and a filtered signal 236. Eventually, such filter stage 220 helps correct the difference to exactly or approximately zero (i.e., corrects the error to zero). Thus, in one embodiment, the transfer function of the filter stage may be an integrator – $H(s)=1/s$. A

filter output signal 225 is sent to the encoder stage 230. In another embodiment, the filter stage 220 may be a second order element.

The encoder stage 230 of one embodiment may modulate the filter output signal 225 (which in this embodiment may be in the form of a pulse code modulated signal) into a pulse width modulated signal 235. The encoder stage 230 of the embodiment depicted in FIG. 2 includes an oversampling filter 232 and a pulse width modulator 234. The oversampling filter 232 of such an embodiment may be, for example, a first order sigma-delta type modulator. In one example embodiment, the oversampling filter 232 may modulate the 16-bit filter output signal 225 at 44.1 kHz into a 4-bit oversampled signal 227 at 1.411 MHz (i.e., 32 * 44.1kHz, which is also called "32x" oversampling). In other embodiments, the oversampling filter 232 may modulate a wide-bit signal (e.g., 12-24 bits) into a signal of only a few bits (e.g., 2-6 bits). The oversampling filter 232 of such an embodiment may be implemented, for example, in a complementary metal oxide semiconductor (CMOS) process.

A sigma-delta modulator 232 of one embodiment may be able to express an amplitude at each sample over a small number of bits, while a pulse width modulator 234 may be able to express an amplitude at each cycle over a short amount of time. The sigma-delta modulator 232 may be very accurately representing the signal with a certain noise characteristic by generating the 4 bits at precise times. However, an unaugmented output signal generated by a pulse width modulator that uses an intermediate sigma-delta modulator to generate the pulse widths in each period may be unsatisfactory or undesirable in certain instances because the output signal may contain a significant amount of distortion. Such distortion is thought to be caused, at least in part, by the

inability of a pulse width modulator to render a sample from the sigma-delta modulator at a precise time.

Mathematically, it is necessary for the bits output from the sigma-delta modulator 232 of one embodiment to be considered as being a good sample at the exact time of the clock that created them. However, although a pulse width modulator 234 may be accurate, it may not be able to maintain this precise timing. For example, if the output of the pulse width modulator 234 is high for the first quarter of the period, a signal level of ¼ is represented. If the output of the pulse width modulator 234 is high for the last quarter of the period though, the signal level is also represented as ¼. Although both of these pulse modulator 234 states represent the same signal level (i.e., ¼ of the signal value), they do so at different times. This inability of the pulse width modulator 234 of one embodiment to render the sigma-delta sample at a precise time is thought to be, at least in part, the cause of distortion introduced by certain sigma-delta-to-pulse-width-modulator encoding processes.

The pulse width modulator 234 of the embodiment shown in FIG. 2 converts the oversampled signal 227 (e.g., a 4-bit signal) from a pulse code modulated digital signal into a relatively small range of time values, such as a pulse width modulated digital signal 235. For example, if the stream of 4-bit data were to be used to control the pulse width modulator 234 such that a 4-bit sample represents the value "5," then the output of the pulse width modulator 234 would be in a high state for 5/16 of its period (in general, if 4-bit data is used to encode a value "N," then the output of the pulse width modulator 234 would be a high state for N/16 of its period). In such an embodiment, the pulse width modulator 234 may operate at a clock rate that is 16 times the period of the

oversampled signal 227. This clock rate for the pulse width modulator 234 is M times the rate of the oversampling filter 232 (where M=16, and is the number of levels in the oversampled signal 227). In at least one embodiment, such a clock rate enables a proper variable pulse width output signal to be created.

The signal processing circuit 200 depicted in FIG. 2 also includes a feedback path. As shown in FIG. 2, the pulse width modulated signal 235 is fed into a digital filter 240 before being combined with (and in this case, subtracted from) the digital input signal 205 at a summing point 210. In this way, the error signal that is fed to the filter stage 220 is the difference between the digital input signal 205 and a filtered signal 236. The digital filter 240 of the embodiment shown in FIG. 2 operates at the clock rate of the pulse width modulator 234, and therefore is able to sample the pulse width modulated output signal 235 at the same rate as the possible quantizations in time of that output.

For example, if the pulse width modulator 234 of one embodiment is running at a clock rate of 16 MHz, it may be able to process a 4-bit quantity over 16 clock cycles. To do so, this pulse width modulator 234 will expect to be provided with a 4-bit quantity at a clock rate of 1 MHz, and then over the next 16 clock cycles (i.e., over the next microsecond before the pulse width modulator 234 processes the next sample), the pulse width modulator 234 generates a pulse width modulated digital signal 235. If the digital filter 240 is operating at the same rate as the pulse width modulated quantizations in time are being received (in this example, a rate of 16 MHz), the digital filter 240 is able to sample every piece of mathematical information present in the pulse width modulated output signal 235. In particular, the digital filter 240 will receive a

sample of every one of the possible positions in time of the pulse width modulated output signal 235, thereby allowing the digital filter 240 to measure the pulse width modulated output signal 235 with no error. Although the digital filter 240 of such an embodiment is not able to appreciate anything happening faster than its clock rate, no information is lost because the pulse width modulator 234 is also not able to change faster than this same clock rate. In this way, the digital filter 240 of one embodiment is able to capture every one of the bits of the pulse width modulated output signal 235.

The digital filter 240 of one embodiment is also able to resynthesize the output signal 235 into a wide-bit (e.g., 16-bit) representation of the output signal 235 to create a filtered signal 236, which is a pulse code modulated signal of the same bit width and clock rate as the digital input signal 205. This filtered signal 236 can then be subtracted from the digital input signal 205 to form an error signal. In one embodiment, the digital filter 240 uses a digital filter design to resynthesize the output signal 235 to form a wide-bit filtered signal 236. This digital filter 240 may be an integrator or recursive averager such as, for example, a simple IIR single pole filter (e.g., $y(n) = y(n-1) + a(x(n) - y(n-1))$, where "a" is a scaling factor such as $1/(2^{\wedge}9)$).

Although the embodiment shown in FIG. 2 includes a closed loop feedback path, it is to be understood that equivalent embodiments using, for example, a feed-forward path or other open loop circuit, may also be implemented.

The closed loop response of the embodiment shown in FIG. 2 is such that distortion from the encoder stage 230 is suppressed, and a number of favorable performance characteristics may be realized. For example, an embodiment of the present invention may exhibit a modulation depth of up to –1 db in the audio frequency band.

In addition, an embodiment of the present invention may suppress errors in the pulse width modulation process such that THD is reduced to about 90-100 db for certain audio equipment applications. The embodiment shown in FIG. 2 is also able to suppress noise from oversampling filter 232. In particular, in an embodiment where the filter stage 220 is an integrator, the oversampling filter 232 is a first order sigma-delta modulator and the digital filter 240 is a first order filter, open loop noise introduced by the sigma-delta modulator 232 may be shaped to a first order (i.e., the noise goes down by 20 db per decade). However, the closed loop response of such an embodiment may suppress this noise by two more orders (i.e., one order from the filter stage 220 element and one order from the digital filter 240 element). In this way, such an embodiment may suppress noise from the oversampling filter 232 to the third order or higher (i.e., the noise falls by 60 db or more per decade).

FIG. 3 shows a block diagram of a digital power amplification system 300 according to an embodiment of the invention. The embodiment shown in FIG. 3 includes a signal processor 200 (as shown, for example, in FIG. 2), a binary power amplifier 320 and a demodulation filter 330. In this embodiment, a digital input signal 205 is sent through the signal processor 200 to obtain a pulse width modulated signal 235. The pulse width modulated signal 235, which in the depicted embodiment is in the form of a rectangular wave, may then be sent to a binary power amplifier 320 where the digital signal 235 is amplified to produce an amplified rectangular wave output 325. In one embodiment, the binary power amplifier 320 may be a Class-D type switching power amplifier that includes, for example, MOSFETs. However, a binary power amplifier 320

of other embodiments of the present invention may include any of a variety of switch configurations and power levels.

In the embodiment depicted in FIG. 3, the amplified rectangular wave output 325 is filtered by a demodulation filter 330 to create an amplified analog output signal 335, which may be suitable for transmission to one or more speakers. In one embodiment, the demodulation filter 330 may be a simple RC filter.

FIGS. 4a and 4b show block diagrams of a method of modulating and amplifying a digital signal according to an embodiment of the present invention. In such an embodiment, a digital input signal 205 is received from, for example, a CD or DVD reader (step 405). The input signal 205 is then oversampled using, for example, a first order sigma-delta modulator (step 410). In such an embodiment, this oversampling converts a wide-bit signal (e.g., 16 bits) into a narrow-bit signal (e.g., 4 bits) that is provided at a faster sampling rate.

Step 415 of FIG. 4a shows a second modulation stage. In the embodiment depicted in FIGS. 4a and 4b, the second modulation stage translates a small range of amplitude values (e.g., an oversampled pulse code modulated signal 227) into a small range of time values (e.g., a pulse width modulated signal) that are provided at a particular clock rate. Then, the pulses in time are measured in the digital domain at a clock rate equal to the clock rate at which the pulses in time have been provided. Step 420 of FIG. 4a depicts this step, and in particular, shows a technique of filtering the pulse width modulated digital signal 235 by integrating or recursively averaging the signal, and converting it into, for example, a 16-bit pulse code modulated signal at 44.1 kHz. In one embodiment, the pulse width modulated digital signal 235 is sampled by a digital filter

240 at the same clock rate as the clock rate that the pulse width modulated digital signal 235 is made.

As shown in FIG. 4a, the digital input signal 205 may be combined with a digital feedback signal which is, for example, a negative filtered signal 236 (step 425). Step 430 depicts a filtering technique (e.g., an integration or recursive averaging process) for gradually correcting any error between the filtered signal 236 and the digital input signal 205.

Next, the corrected digital output signal 235 may be amplified, as shown in step 435 of the embodiment shown in FIG. 4b. Step 440 of one embodiment is a low pass filter process which converts the amplified digital pulse width modulated output signal 235 into an analog signal. This filter process achieves a digital-to-analog conversion by essentially integrating the area beneath the square wave to produce an analog output.

FIG. 5a shows a simplified integrated circuit chip 501 of an embodiment of the present invention. In the embodiment shown in FIG. 5a, the integrated circuit chip 501 includes two signal processors 200-1, 200-2, one for each of two output channels. Such a chip 501 may also include a master clock 510, one or more input buffers 520, and one or more output buffers 530-1, 530-2.

The embodiment shown in FIG. 5b is an integrated circuit chip 551 that includes eight signal processors 200-1 to 200-8, which may be used in a surround sound system to produce eight channels of output. This chip 551 may also have a master clock 560, one or more input buffers 570, and one or more output buffers 580.

The output frequency of certain audio equipment applications is expected to be in the range of 350 kHz to 800 kHz. If a sampling frequency of a DVD player is about 48 kHz, the sampling frequency of integrated circuit chips 501, 551 of certain embodiments of the present invention may be 12.288 MHz (i.e., 48 kHz*256). Master clocks 510, 560 for certain embodiments of integrated circuit chips 501, 551 may then operate at 12.288 MHz to produce outputs with frequencies of about 768 kHz. In such embodiments, both the pulse width modulators 234 and the digital filters 240 of the signal processors 200-1 to 200-N may operate at 12.288 MHz.

FIG. 6 shows a portable audio player 600 according to one embodiment of the present invention. This portable player 600 may include a digital power amplification system 300, one or more digital audio signal sources, and one or more output devices such as a headphone jack 610 or a speaker 612-1. In accordance with certain embodiments of the present invention, the digital audio signal source may include one or more of the following: a digital receiver 602 (e.g., a radio signal receiver), a memory medium reader such as an optical disk reader 604 (e.g., a CD reader), or a memory device for storage of a digital audio file 606 (e.g., an MPEG file).

FIGS. 7a-7d show a computer code listing for certain Verilog modules that implement one embodiment of the present invention. In these modules, "Clk" is a clock signal that may run at a multiple of an audio data rate, for example 24 MHz is approximately 512 * 44.1 kHz. "Clken" is a clock enable signal that may be tied high, thus enabling every clock. "Reset" is an asynchronous reset, and will typically return to a low level after system initialization. "Phase" is a 5-bit counter in this example, and is expected to advance on each edge of the clock. "Phase" is used in the PWM cell to

generate the PWM output bit. "In" is the input data, typically audio data in a 16 bit-word. The variable "pwm" is the output bit in a pulse width modulated format generated by these modules.

FIG. 8 is a frequency response plot generated by a computer model of one embodiment of the present invention. In this modeled embodiment, the filter stage 220 is an integrator, the oversampling filter 232 is a first order sigma-delta modulator having 16 levels, and the pulse width modulator 234 is running at a clock rate that is 16 times the clock rate of the oversampling filter 232. The digital input signal 205 provided to the signal processor 200 of this modeled embodiment is 24 bits wide (as is the wide-bit filtered signal 236). The digital filter 240 of this modeled embodiment is a first order filter running at a clock rate of 27 MHz. As shown in FIG. 8, the modeled embodiment has favorable distortion and noise characteristics for certain applications or users, e.g., certain audio equipment applications.

FIG. 9 is a frequency response plot generated by a computer model of another embodiment of the present invention. In this second modeled embodiment, the filter stage 220 is a second order filter, the oversampling filter 232 is a first order sigma-delta modulator having 32 levels, and the pulse width modulator 234 is running at a clock rate that is 32 times the clock rate of the oversampling filter 232. The digital input signal 205 provided to the signal processor 200 of this modeled embodiment is 24 bits wide (as is the wide-bit filtered signal 236). The digital filter 240 of this second modeled embodiment is a first order filter running at a clock rate of 27 MHz. As shown in FIG. 9, the modeled embodiment generates essentially no distortion and very low noise up to about 200 kHz.

FIG. 10 is a frequency response plot generated by a signal processor 200 implemented on a field programmable gate array (FPGA) board that is measured using an audio measurement system. In this signal processor 200, the filter stage 220 is a second order filter, the oversampling filter 232 is a first order sigma-delta modulator having 32 levels, the and the pulse width modulator 234 is running at a clock rate that is 32 times the clock rate of the oversampling filter 232. The digital input signal 205 provided to the signal processor 200 is 24 bits wide (as is the wide-bit filtered signal 236). The digital filter 240 of this signal processor 200 is a first order filter running at a clock rate of 27 MHz. As shown in FIG. 10, the THD of such a signal processor 200 (of which the output has been filtered with an RC filter) is about 90 db.

Although illustrative embodiments and example methods have been shown and described herein in detail, it should be noted and will be appreciated by those skilled in the art that there may be numerous variations and embodiments which may be equivalent to those explicitly shown and described. For example, the scope of the present invention may not necessarily be limited in all cases to execution of the aforementioned steps in the order discussed. Unless otherwise specifically stated, the terms and expressions have been used herein as terms and expressions of description, not of limitation. Accordingly, the invention is not to be limited by the specific illustrated and described embodiments and examples (or terms or expressions used to describe them), but only by the scope of the amended claims.